AMENDMENTS TO THE CLAIMS

Claim 1 (Currently Amended) A simulation apparatus ~~that is intended for~~ for simulating a very long instruction word processor, said simulation apparatus comprising:

a first simulation unit operable to simulate execution of a group of instructions intended to be simultaneously executed ~~simultaneously~~, and to generate a first simulation result; and

a second simulation unit operable to simulate, based on the first simulation result generated by said first simulation unit, a sequential execution ~~generate a simulation result~~ of ~~the~~ said group of instructions on an instruction-by-instruction basis ~~based on a simulation result generated by the first simulation unit~~, and to generate a second simulation result.

Claim 2 (Currently Amended) The simulation apparatus according to Claim 1, wherein ~~the~~ said second simulation unit is operable to generate ~~generates a~~ the second simulation result by undoing ~~a~~ the simulation of the execution of one of the instructions ~~an instruction included in a~~ from said group of instructions ~~that has just been~~ previously simulated by ~~the~~ said first simulation unit.

Claim 3 (Currently Amended) The simulation apparatus according to Claim 2 further comprising: a display control unit operable to control a display unit to display the second simulation result generated by ~~the~~ said second simulation unit.

Claim 4 (Currently Amended) The simulation apparatus according to Claim 2, wherein ~~the~~ said second simulation unit includes:

a judgment unit operable to judge whether or not an instruction that satisfies a break condition is included in the execution of said group of instructions ~~that has just been~~ previously simulated by ~~the~~ said first simulation ~~unit or not~~;

an indication unit operable to ~~indicate that the~~ direct said first simulation unit to simulate ~~simulates~~ execution of a next group of instructions when ~~it is judged~~ said judgment unit judges that no instruction satisfying the break condition is included in the execution of said group of instructions previously simulated by said first simulation unit;

a determination unit operable to determine that an instruction of said group of instructions ~~as~~ is a stop instruction when ~~it is judged~~ said judgment unit judges that the instruction satisfying the break condition is included; and

a generation unit operable to generate a simulation result by undoing simulations of the execution of the stop instruction and ~~the following~~ subsequent instructions in the execution of said group of instructions ~~that have just been~~ previously simulated.

Claim 5 (Currently Amended) The simulation apparatus according to Claim 1, wherein

~~the~~ said first simulation unit is ~~intended for~~ operable to simulate ~~operations of a~~ pipeline processor that simultaneously executes a plurality of instructions ~~simultaneously~~, and

~~the~~ said simulation apparatus further comprises~~:~~ a display image generation unit operable to generate a display image showing instructions ~~that are~~ included in a pipeline based on the first simulation results generated by ~~the~~ said first simulation unit and the second simulation results generated by said ~~the~~ second simulation unit.

Claim 6 (Currently Amended) The simulation apparatus according to Claim 5, wherein the display image contains a representation of an instruction ~~that is~~ included in every stage of the pipeline.

Claim 7 (Currently Amended) The simulation apparatus according to Claim 1, wherein

~~the~~ said first simulation unit is operable to simulate ~~simulates~~, on a cycle-by-cycle basis, ~~operations of~~ a pipeline processor that simultaneously executes a plurality of instructions ~~simultaneously~~,

~~the~~ said simulation apparatus further comprises~~:~~

an acception unit operable to accept a user ~~operation that indicates one of~~ instruction for indicating a step to be executed ~~execution performed~~ on the ~~an~~ instruction-by-instruction basis and for indicating a step to be executed ~~execution performed~~ on the ~~a~~ cycle-by-cycle basis; and

a display image generation unit operable to generate a display image ~~that shows~~ showing ~~a~~ the second simulation result generated ~~on an instruction-by-instruction basis~~ by ~~the~~ said second simulation unit when ~~a~~ the user ~~operation~~ instruction that indicates ~~a~~ the step to be executed ~~execution performed~~ on the ~~an~~ instruction-by-instruction basis is accepted by said acception unit, and to generate a display image ~~that shows~~ showing a simulation result generated on the ~~a~~ cycle-by-cycle basis by ~~the~~ said first simulation unit when ~~a~~ the user instruction ~~operation~~ that indicates ~~a~~ the step to be executed ~~execution performed~~ on ~~a~~ the cycle-by-cycle basis is accepted by said acception unit.

Claim 8 (Currently Amended) The simulation apparatus according to Claim 7, wherein the display image contains a representation of each instruction ~~that is~~ included in ~~a~~ the pipeline.

Claim 9 (Currently Amended) The simulation apparatus according to Claim 7, wherein the display image contains a representation of each instruction~~s that is~~ included in every stage of ~~a~~ the pipeline.

Claim 10 (Currently Amended) The simulation apparatus according to Claim 1, wherein ~~the~~ said first simulation unit includes:

a hold unit operable to hold first data ~~showing~~ indicating resources of the very long instruction word processor;

a storage unit operable to store a copy of the first data in ~~the~~ a memory unit as second data; and

a first simulator ~~that updates~~ operable to update the first data by simulating an execution of a single group of instructions after said storage unit stores ~~storing~~ the copy of the first data, ~~and~~

wherein ~~the~~ said second simulation unit is operable to obtain ~~obtains~~ the second simulation results of the execution of said group of instructions on ~~an~~ the instruction-by-instruction basis based on the first data and the second data.

Claim 11 (Currently Amended) The simulation apparatus according to Claim 10, wherein

~~the~~ said storage unit ~~stores~~ is operable to store register data ~~of a register set~~ in the memory unit as the second data, and

~~the~~ said second simulation unit ~~reconstructs~~ is operable to reconstruct data ~~of the~~ indicating a resource of the very long instruction word processor before executing ~~a~~ the simulation of the instruction of ~~the~~ said group of instructions on ~~an~~ the instruction-by-instruction basis.

Claim 12 (Currently Amended) The simulation apparatus according to Claim 11, wherein ~~the~~ said storage unit ~~further stores~~ is operable to store memory data, before memory writing, in ~~the~~ said hold unit, and to store the memory data so ~~in a way~~ that ~~said~~ the memory data is contained in the second data when a memory write instruction is included in ~~the~~ said group of instructions.

Claim 13 (Currently Amended) The simulation apparatus according to Claim 10, wherein ~~the~~ said second simulation unit ~~includes~~ further comprises:

a judgment unit operable to judge whether or not an instruction that satisfies a break condition is included in the execution of said group of instructions ~~that has just been~~ previously simulated by ~~the~~ said first simulation unit ~~or not~~;

an indication unit operable to ~~indicate that the~~ direct said first simulation unit to simulate ~~simulates~~ execution of a next group of instructions when ~~it is judged~~ said judgment unit judges that no instruction satisfying the break condition is included in the execution of said group of instructions previously simulated by said first simulation unit; and

a determination unit operable to determine that an instruction ~~that satisfies the break condition as~~ is a stop instruction when ~~it is judged~~ said judgment unit judges that the instruction satisfying the break condition is included.

Claim 14 (Currently Amended) The simulation apparatus according to Claim 13, wherein ~~the~~ said determination unit ~~determines~~ is operable to determine that an

instruction next to a present stop instruction ~~as~~ is a break condition in ~~the~~ a step of execution of a simulation performed on an instruction-by-instruction basis.

Claim 15 (Currently Amended) The simulation apparatus according to Claim 13, wherein ~~the~~ said second simulation unit further ~~includes:~~ comprises a reconstruction unit operable to reconstruct, based on the first data and the second data, data ~~of~~ indicating the resources of the very long instruction word processor, on a condition that execution of previous instructions, up to an instruction just ~~before~~ prior to the stop instruction determined by ~~the~~ said determination unit, ~~are~~ has been simulated.

Claim 16 (Currently Amended) The simulation apparatus according to Claim 13, wherein ~~the~~ said second simulation unit further ~~includes:~~ comprises a reconstruction unit operable to reconstruct, based on the first data and the second data, data ~~of~~ indicating the resources of the very long instruction word processor, on a condition that execution of previous instructions, up to the stop instruction determined by ~~the~~ said determination unit, ~~are~~ has been simulated.

Claim 17 (Currently Amended) The simulation apparatus according to Claim 16, wherein

~~the~~ said first simulator ~~generates~~ is operable to generate update information indicating ~~showing~~ resources of the very long instruction word processor to be changed by each instruction of ~~the~~ said group of instructions, and

~~the~~ said reconstruction unit ~~reconstructs~~ is operable to reconstruct the data ~~of~~ from the resources of the very long instruction word processor that correspond~~ing~~ to a result of a sequential execution ~~results~~ of the instructions ~~up to each instruction of~~ ~~the~~ said group of instructions according to the first data, the second data, and the update information.

Claim 18 (Currently Amended) The simulation apparatus according to Claim 10, wherein

~~the~~ said first simulator ~~simulates~~ is operable to simulate an execution of the group of instructions on a cycle-by-cycle basis of pipeline processing, ~~the first simulator being intended for the very long instruction word processor that executes the pipeline processing~~, and

the simulation apparatus ~~further counts the number~~ is operable to count a quantity of execution cycles in the simulation for every group of instructions.

Claim 19 (Currently Amended) The simulation apparatus according to Claim 18, wherein

the very long instruction word processor to be simulated ~~has~~ includes a cancellation unit ~~for canceling~~ operable to cancel an execution of an instruction within a plurality of instructions to be simultaneously executed ~~simultaneously~~, and

~~the~~ said first simulator ~~simulates the~~ is operable to simulate said cancellation unit.

Claim 20 (Currently Amended) The simulation apparatus according to Claim 18, wherein

~~the~~ said first simulator ~~further simulates~~ is operable to simulate a delay cycle ~~as~~ according to a delay instruction that causes a delay cycle in an execution stage of the very long instruction word processor to be simulated, and

~~the~~ said reconstruction unit ~~generates~~ is operable to reconstruct data ~~of~~ indicating the resources of the very long instruction word processor that correspond~~ing~~ to a simulation result from simulating ~~of a~~ the delay cycle ~~instruction~~ according to update information ~~on~~ for the delay instruction.

Claim 21 (Currently Amended) The simulation apparatus according to Claim 20, wherein ~~the~~ said reconstruction unit ~~apparatus further generates~~ is operable to generate data ~~of~~ indicating the resources of the very long instruction word processor that correspond~~ing~~ to a simulation result of simulating an output dependency instruction according to the update information ~~on~~ for the delay instruction and according to the update information ~~on~~ for the output dependency instruction ~~as to the output dependency~~

~~instruction~~ that has an output dependency in the same group of instructions ~~with~~ as the delay instruction.

Claim 22 (Currently Amended) A simulation method ~~that is intended~~ for simulating a very long instruction word processor, said simulation method comprising:

performing a ~~the~~ first simulation comprising ~~step of~~ simulating execution of a group of instructions comprising a plurality of instructions intended to be simultaneously executed ~~simultaneously~~, and generating a first simulation result of said first simulation; and

performing a ~~the s~~econd simulation comprising ~~step of generating a simulation result~~ simulating, based on the first simulation result, a sequential execution of ~~the~~ said group of instructions on an instruction-by-instruction basis ~~based on a simulation result in the first step~~ and generating a second simulation result of said second simulation.

Claim 23 (Currently Amended) A computer-readable recording medium which stores a program for ~~having~~ executing on a computer ~~execute~~ a simulation of a very long instruction word processor, the program ~~has~~ causing the computer to execute a method comprising ~~the following steps~~:

performing a ~~the~~ first simulation comprising ~~step of~~ simulating execution of a group of instructions comprising a plurality of instructions intended to be simultaneously executed ~~simultaneously~~, and generating a first simulation result of said first simulation; and

performing a ~~the s~~econd simulation comprising ~~step of generating a simulation result~~ simulating, based on the first simulation result, a sequential execution of ~~the~~ said group of instructions on an instruction-by-instruction basis ~~based on a simulation result in the first step~~ and generating a second simulation result of said second simulation.